CLAIM AMENDMENTS

In the Claims

This listing of the claims will replace all prior versions, and listing, of claims in the application or previous response to office action:

1. **(Currently Amended)** A ~~**Semiconductor**~~ **semiconductor** device comprising:
- a semiconductor substrate having a top and a bottom surface,
- first and second insulating ~~**layer**~~ **layers** deposited on the top surface of said substrate,
- a runner arranged on top of the second insulator layer,
- a backside metal layer deposited on the bottom surface of the substrate,
- a first via structure extending from the bottom surface of the substrate to the top of the first insulating layer between the backside layer and the runner,~~**and**~~
- a second via structure extending from the top of the first insulating layer to the top of the second insulating layer between the first via and the runner**, and**
- barrier metal layers arranged between the first and second vias, between the runner and the second via, and between the first via and the backside metal layer.

2. **(Canceled)**

3. **(Currently Amended)** The ~~**Semiconductor**~~**semiconductor** device as claimed in Claim 1, wherein the second via has a smaller footprint than the first via and a plurality of second vias are arranged between the first via and the runner.

4. **(Currently Amended)** The ~~**Semiconductor**~~ **semiconductor** device as claimed in Claim ~~**2**~~**1**, wherein said barrier metal layer between the first and second ~~**via**~~ **vias** has a cross-sectional profile of a saucer.

5. **(Currently Amended)** The ~~**Semiconductor**~~ **semiconductor** device as claimed in Claim 4, wherein the bottom barrier metal layer comprises side walls that enclose said via.

6. **(Currently Amended)** The ~~Semiconductor~~ semiconductor device as claimed in Claim 4, wherein the barrier metal layer between the first via and the second via comprises side walls that are spaced apart from said via.

7. **(Currently Amended)** The ~~Semiconductor~~ semiconductor device as claimed in Claim ~~2~~1, wherein the barrier metal layer between the first via and the second via consists of Titanium-Titanium nitride.

8. **(Currently Amended)** The ~~Semiconductor~~ semiconductor device as claimed in Claim ~~2~~1, wherein the barrier metal layer between the runner and the second via and the barrier metal layer between the backside layer and the first via consist of Titanium-Platinum.

9. **(Currently Amended)** The ~~Semiconductor~~ semiconductor device as claimed in Claim 1, wherein the second via is filled with tungsten.

10. **(Currently Amended)** The ~~Semiconductor~~ semiconductor device as claimed in Claim ~~13~~ 1, wherein the first via is filled with Tungsten or copper.

11. **(Currently Amended)** The ~~Semiconductor~~ semiconductor device as claimed in Claim 1, wherein the substrate comprises a p+ substrate and p- epitaxial layer.

12. **(Currently Amended)** The ~~Semiconductor~~ semiconductor device as claimed in Claim 1, wherein first and second via structures are arranged between a first and second stage of an integrated device for electromagnetic and /or thermal de-coupling.

13. **(Currently Amended)** The ~~Semiconductor~~ semiconductor device as claimed in Claim 12, wherein the first stage is an input transistor stage and the second stage is a power transistor output stage.

14. **(Currently Amended)** The ~~Semiconductor~~ semiconductor device as claimed in Claim 3, wherein the first via structure is extended in such a way that it at least partly surround a first device formed within said semiconductor device for electromagnetic and /or thermal de-coupling.

15. **(Currently Amended)** The ~~Semiconductor~~ semiconductor device as claimed in Claim 14, wherein the first via structure is extended in such a way that it at least completely surrounds said first device.

16. **(Currently Amended)** The ~~Semiconductor~~ semiconductor device as claimed in Claim 14, wherein the first and second via structures are extended to form a grid including cells in which certain semiconductor devices are formed.

17. **(Currently Amended)** The ~~Semiconductor~~ semiconductor device as claimed in Claim 14, wherein said first device includes an active semiconductor structure.

18. **(Currently Amended)** The ~~Semiconductor~~ semiconductor device as claimed in Claim 14, wherein said first device includes a passive semiconductor structure.

19. **(Currently Amended)** The ~~Semiconductor~~ semiconductor device as claimed in Claim 14, wherein the first device is shielded from a second device and the first device is coupled with the second device through at least one electrical coupling.

20. **(Currently Amended)** The ~~Semiconductor~~ semiconductor device as claimed in Claim 19, wherein the second via structure comprises an opening for providing a passageway for the electrical coupling.

21. **(Currently Amended)** The ~~Semiconductor~~ semiconductor device as claimed in Claim 19, wherein the electrical coupling is arranged in a first or second metal layer.

22. **(Currently Amended)** The ~~Semiconductor~~ semiconductor device as claimed in Claim 1, wherein the first and second via structures are arranged within a field effect transistor structure having a source region, a drain region and a gate, in such a way that the first via couples the source region with the backside layer.

23. **(Currently Amended)** The ~~Semiconductor~~ semiconductor device as claimed in Claim ~~22~~67, further comprising at least one drain runner arranged on top of the first and/or second oxide layer above said drain region and on one side of the first and second via structures, and at least one gate runner arranged on top of the first and/or second oxide layer on the other side of the first and second via structures.

24.-66. (Canceled)

67. **(NEW)** A semiconductor device comprising:
- a semiconductor substrate having a top and a bottom surface,
- first and second insulating layers deposited on the top surface of said substrate,
- a runner arranged on top of the second insulator layer,
- a backside metal layer deposited on the bottom surface of the substrate,
- a first via structure extending from the bottom surface of the substrate to the top of the first insulating layer between the backside layer and the runner,
- a second via structure extending from the top of the first insulating layer to the top of the second insulating layer between the first via and the runner, wherein the first and second via structures are arranged within a field effect transistor structure having a source region, a drain region and a gate, in such a way that the first via couples the source region with the backside layer.

68. **(NEW)** The semiconductor device as claimed in Claim 67, further comprising barrier metal layers arranged between the first and second vias, between the runner and the second via, and between the first via and the backside metal layer.

69. (NEW) The semiconductor device as claimed in Claim 67, wherein the second via has a smaller footprint than the first via and a plurality of second vias are arranged between the first via and the runner.

70. (NEW) The semiconductor device as claimed in Claim 67, wherein said barrier metal layer between the first and second vias has a cross-sectional profile of a saucer.

71. (NEW) The semiconductor device as claimed in Claim 70, wherein the bottom barrier metal layer comprises side walls that enclose said via.

72. (NEW) The semiconductor device as claimed in Claim 70, wherein the barrier metal layer between the first via and the second via comprises side walls that are spaced apart from said via.

73. (NEW) The semiconductor device as claimed in Claim 67, wherein the barrier metal layer between the first via and the second via consists of Titanium-Titanium nitride.

74. (NEW) The semiconductor device as claimed in Claim 67, wherein the barrier metal layer between the runner and the second via and the barrier metal layer between the backside layer and the first via consist of Titanium-Platinum.

75. (NEW) The semiconductor device as claimed in Claim 67, wherein the second via is filled with tungsten.

76. (NEW) The semiconductor device as claimed in Claim 67, wherein the first via is filled with Tungsten or copper.

77. (NEW) The semiconductor device as claimed in Claim 67, wherein the substrate comprises a p+ substrate and p- epitaxial layer.

78. (NEW) The semiconductor device as claimed in Claim 67, wherein first and second via structures are arranged between a first and second stage of an integrated device for electromagnetic and /or thermal de-coupling.

79. (NEW) The semiconductor device as claimed in Claim 78, wherein the first stage is an input transistor stage and the second stage is a power transistor output stage.

80. (NEW) The semiconductor device as claimed in Claim 69, wherein the first via structure is extended in such a way that it at least partly surround a first device formed within said semiconductor device for electromagnetic and /or thermal de-coupling.

81. (NEW) The semiconductor device as claimed in Claim 80, wherein the first via structure is extended in such a way that it at least completely surrounds said first device.

82. (NEW) The semiconductor device as claimed in Claim 80, wherein the first and second via structures are extended to form a grid including cells in which certain semiconductor devices are formed.

83. (NEW) The semiconductor device as claimed in Claim 80, wherein said first device includes an active semiconductor structure.

84. (NEW) The semiconductor device as claimed in Claim 80, wherein said first device includes a passive semiconductor structure.

85. (NEW) The semiconductor device as claimed in Claim 80, wherein the first device is shielded from a second device and the first device is coupled with the second device through at least one electrical coupling.

86. (NEW) The semiconductor device as claimed in Claim 85, wherein the second via structure comprises an opening for providing a passageway for the electrical coupling.

87. **(NEW)** The semiconductor device as claimed in Claim 85, wherein the electrical coupling is arranged in a first or second metal layer.